What is claimed is:

1. A peripheral or memory device having a bus, and a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding signals in a first format;

a second bus decoder circuit coupled to the bus for decoding signals in a second format;

a first bus snoop circuit coupled to the bus;

a second bus snoop circuit coupled to the bus;

a switch coupled to the first bus snoop circuit for receiving a first bus detect signal therefrom, and the switch coupled to the second bus snoop circuit for receiving a second bus detect signal therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the first and second detect signals.

2. The device of claim 1, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.

3. A peripheral or memory device comprising:

a bus;

a micro-controller; and

a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding signals in a first format;

a second bus decoder circuit coupled to the bus for decoding signals in a second format;

a switch coupled to the micro-controller for receiving a bus select signal therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of

the bus select signal.

4. The device of claim 3, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.

5. A peripheral or memory device comprising:

a bus;

a pin; and

a bus switching circuit that comprises:

a first bus decoder circuit coupled to the bus for decoding signals in a first format;

a second bus decoder circuit coupled to the bus for decoding signals in a second format;

a switch coupled to the micro-controller for receiving a bus select signal therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the bus select signal.

6. The device of claim 5, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.

7. A peripheral or memory device comprising:

a bus;

a first bus decoder circuit coupled to the bus for decoding a first type of bus signal;

a second bus decoder circuit coupled to the bus for decoding a second type of bus signal;

means for detecting whether the bus is a first type of bus or a second type of bus, the detecting means outputting a select signal;

a switch coupled to the detecting means for receiving the select signal therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the select signal.

8. The device of claim 7, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.

9. The device of claim 7, wherein the detecting means comprises:

a first bus snoop circuit coupled to the bus;

a second bus snoop circuit coupled to the bus; and

wherein the switch is coupled to the first bus snoop circuit for receiving a first bus detect signal therefrom, and the switch is coupled to the second bus snoop circuit for receiving a second bus detect signal therefrom.

10. The device of claim 7, wherein the detecting means comprises a micro-controller.

11. The device of claim 7, wherein the detecting means comprises a pin.

12. A peripheral or memory device comprising:

a bus;

a first bus decoder circuit coupled to the bus for decoding a first type of bus signal;

a second bus decoder circuit coupled to the bus for decoding a second type of bus signal;

a detecting circuit that determines whether the bus is a first type of bus or a second type of bus, the detecting circuit outputting a select signal;

a switch coupled to the detecting circuit for receiving the select signal therefrom; and

wherein the switch is coupled to the first bus decoder circuit for providing a first bus enable signal thereto, and the switch is coupled to the second bus decoder circuit for providing a second bus enable signal thereto, depending on the nature of the select signal.

13. The device of claim 12, wherein the first bus decoder circuit is an ISA bus decoder circuit, and the second bus decoder circuit is an LPC bus decoder circuit.

14. The device of claim 12, wherein the detecting circuit comprises:

a first bus snoop circuit coupled to the bus;

a second bus snoop circuit coupled to the bus; and

wherein the switch is coupled to the first bus snoop circuit for receiving a first bus detect signal therefrom, and the switch is coupled to the second bus snoop circuit for receiving a second bus detect signal therefrom.

15. The device of claim 12, wherein the detecting means comprises a micro-controller.

16. The device of claim 12, wherein the detecting means comprises a pin.